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(74) Agents Marks & Clerk

(54) **A noise limiter circuit**

(57) A noise limiter circuit comprises a series circuit of a differentiator (18), an amplitude limiter (19), an integrator (20), and a threshold voltage generating circuit (10) which controls the threshold voltages of the amplitude limiter. The threshold voltage generating circuit includes a level detector (21) which produces an output signal indicative of the magnitude of the input signal of the noise limiter circuit, and a voltage control circuit (22) which produces first and second threshold voltages in accordance with the output voltage of the level detector. The threshold voltages of the amplitude limiter are so controlled that the limiting range widens as the magnitude of the input signal increases thereby preventing occurrence of undesirable distortion upon receiving an input signal of high amplitude.

Fig. 3

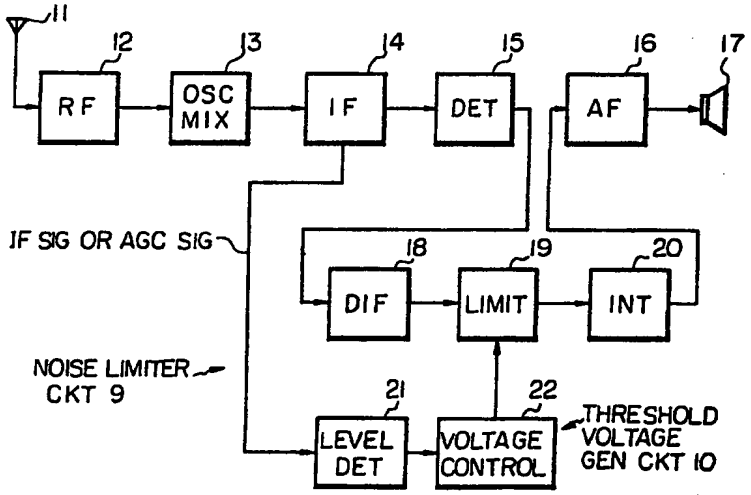


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Fig. 1

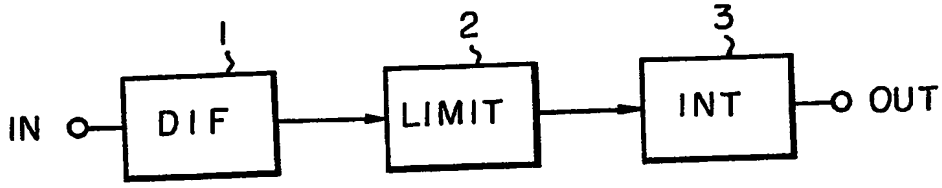



Fig. 2

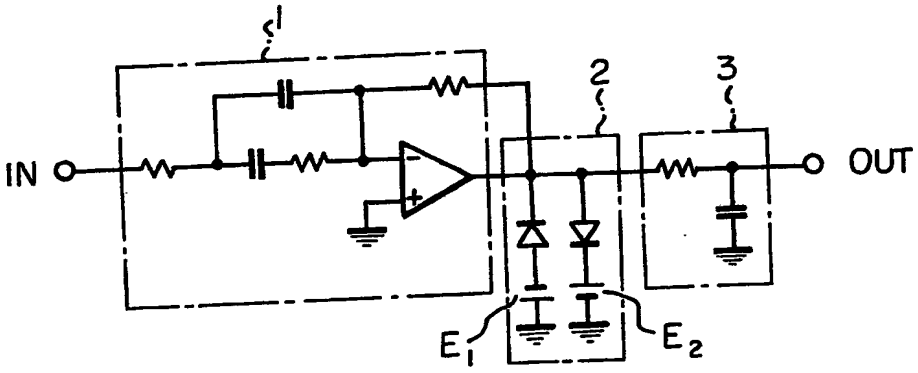


Fig. 3

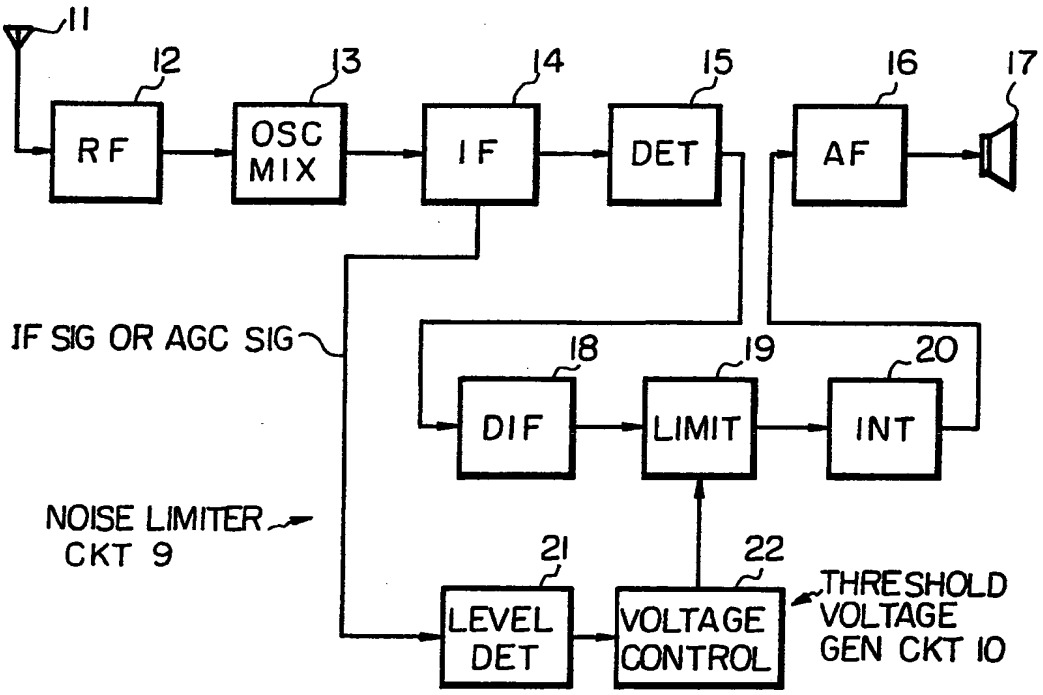

11
12
13
14
15
16
17
RF
OSC MIX
IF
DET
AF
IF SIG OR AGC SIG
18
19
20
DIF
LIMIT
INT
NOISE LIMITER CKT 9
21
22
LEVEL DET
VOLTAGE CONTROL
THRESHOLD VOLTAGE GEN CKT 10

Fig. 4

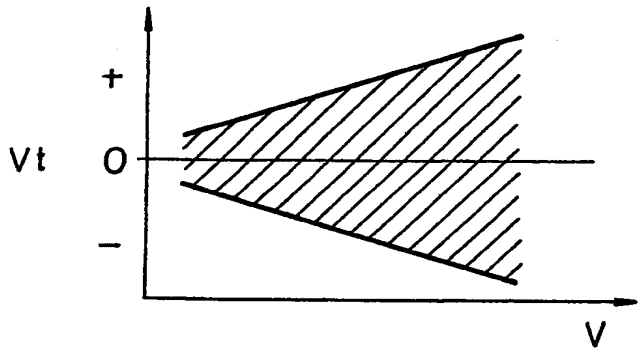
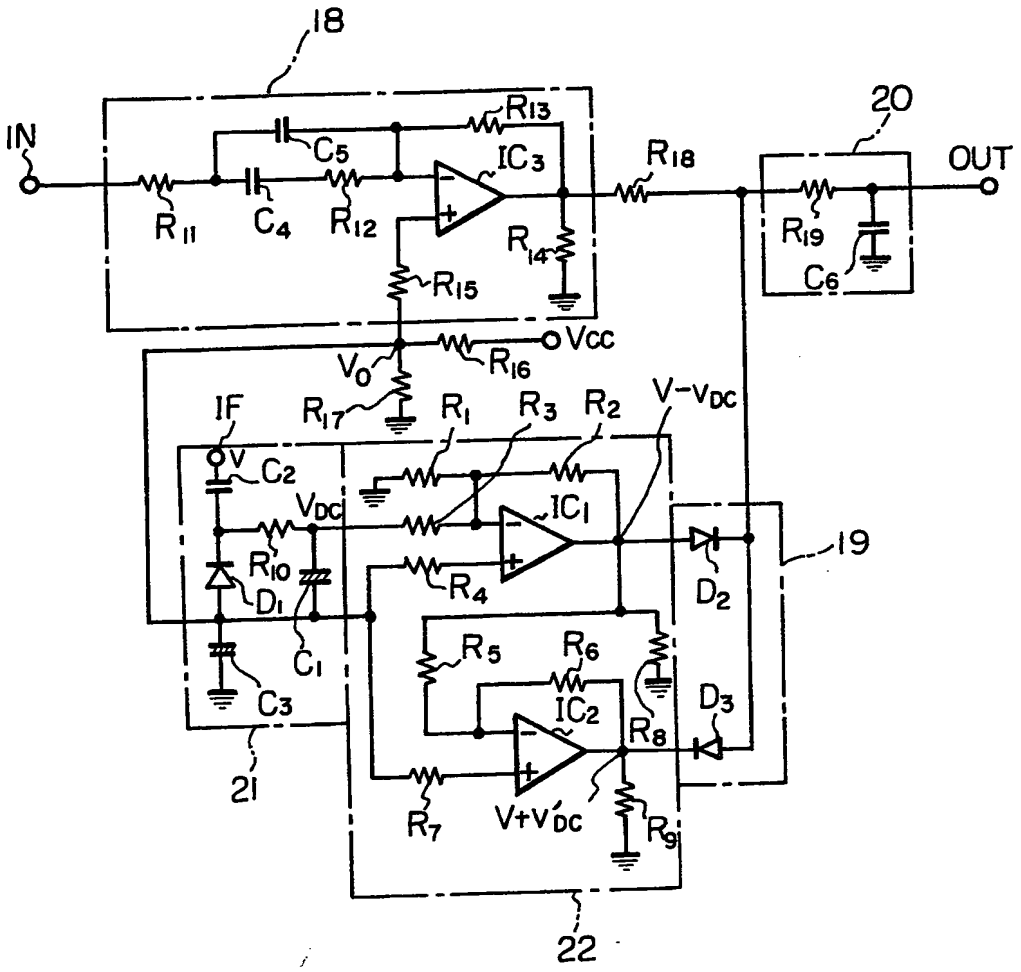

+
Vt
0
−
V

Fig. 5


18
IN
R11
C4
C5
R12
R13
IC3
R14
R15
Vcc
R16
V0
R17
IF
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C2
R1
R3
R2
V-VDC
VDC
IC1
R10
D1
C1
C3
R4
21
R5
R6
IC2
R8
D3
D2
19
R7
V+V'DC
R9
22
R18
20
R19
C6
OUT

Fig. 6A

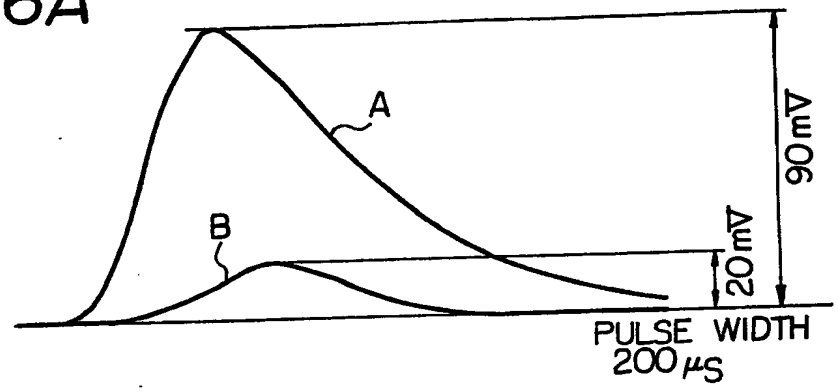



Fig. 6B

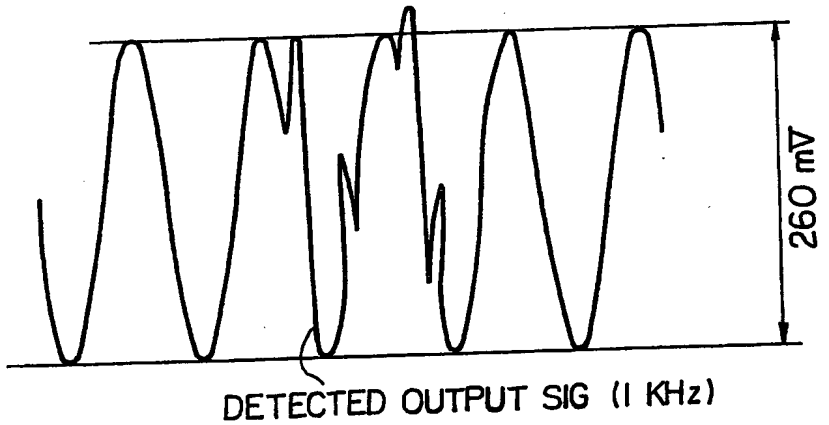
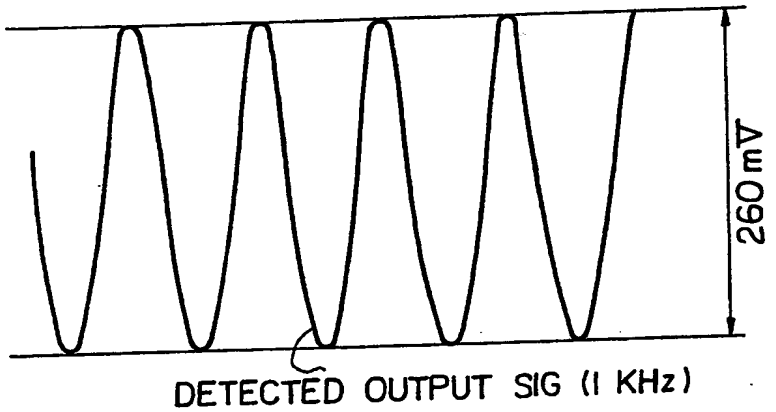



Fig. 6C



SPECIFICATION

**A noise limiter circuit**

This invention generally relates to a noise limiter circuit. More particularly, the present invention relates to such a noise limiter circuit used in a radio receiver for eliminating impulsive noise induced in a radio receiver.

In one of conventional noise limiters for reducing impulsive noise, the frequency and the voltage of the input signal is limited within a predetermined level or range. According to this conventional method of noise suppression, the input signal is applied to a differentiator the output of which is connected to an amplitude limiter. The output of the amplitude limiter is connected to an integrator to reproduce the original input signal. The amplitude limiter limits the amplitude of the differentiated signal so that impulsive noise components are eliminated since the magnitude of the differentiated impulsive noise components is usually greater than that of the differentiated signal components. The differentiated signal applied via the amplitude limiter to the integrator is thus integrated so that the original input signal is obtained at the output of the integrator where this output signal of the integrator does not include the impulsive noise components.

In the above described conventional method, the threshold voltages, i.e. the clipping levels, of the amplitude limiter are so set that the threshold voltages are effective against a differentiated signal corresponding to a noise the magnitude of which is great throughout a wide frequency range (i.e. the product of the frequency amplitude of the noise component is great), such as an impulsive noise, while the threshold voltages are not effective against a differentiated signal corresponding to the signal components. Namely, the impulsive noise component is eliminated while the signal component is transmitted via the noise limiter as is so that the original signal is restored by the integrator.

However, since the threshold voltages of the amplitude limiter are fixedly predetermined, when the magnitude of the input signal (such as a detected signal derived from a receiving signal of a radio receiver) is great, the amplitude of the signal component is also limited by the amplitude limiter so that the output signal of the integrator includes a distortion component.

The present invention has been achieved in order to remove the above mentioned drawback of the conventional noise limiter circuit.

It is therefore, an object of the present invention to provide a noise limiter circuit in which the output signal of the limiter circuit does not include distortion components even though the magnitude of the input signal is relatively great.

Another object of the present invention is to provide such a noise limiter circuit in which the efficiency of noise suppression is high.

A further object of the present invention is to provide such a noise limiter in which the threshold voltages of the amplitude limiter included in the limiter circuit are variable in accordance with the magnitude of the input signal.

According to the present invention, there is provided a noise limiter circuit including: (a) a differentiator responsive to an input signal for producing a differentiated signal; (b) an amplitude limiter responsive to the differentiated signal for limiting the amplitude of the differentiated signal; and (c) an integrator responsive to the output signal of the amplitude limiter for restoring the original input signal where the noise components included in the input signal are suppressed; wherein the improvement comprises: means for providing the amplitude limiter with variable threshold voltages, which are arranged to vary in accordance with the magnitude of the input signal.

These and other objects and features of the present invention will become more readily apparent from the detailed description of the preferred embodiment taken in conjunction with the accompanying drawings in which:

*Figure 1* shows in schematic block diagram form a conventional noise limiter circuit;

*Figure 2* shows in detailed circuit diagram form the conventional noise limiter circuit shown in Figure 1;

*Figure 3* shows in schematic block diagram form a preferred embodiment of a noise limiter circuit according to the present invention;

*Figure 4* is a graphical representation of the variation of the threshold voltages used in the noise limiter circuit shown in Figure 3;

*Figure 5* shows in detailed circuit diagram form of the noise limiter circuit shown in Figure 3, and

*Figure 6A to 6C* are graphical representations of the results of experiments of the noise limiter circuit according to the present invention.

Prior to the description of the preferred embodiment of the noise limiter circuit according to the present invention, the prior art technique will be discussed hereinbelow for a better understanding of the object of the present invention.

Reference is now made to Figure 1 which shows a schematic block diagram of a conventional noise limiter circuit used in an AM (amplitude modulation) radio receiver. In this circuit, the product of the frequency and voltage of the input signal is limited within a predetermined value. The noise limiter includes a differentiator 1, an amplitude limiter 2 and an integrator 3 which are all connected in series. The input signal is applied to the input of the differentiator 1 so that the input signal is differentiated. This differentiated signal is applied to the input of the amplitude limiter where the amplitude of the differentiated signal is limited within a predetermined value or range. The output signal of the amplitude limiter 2 is applied to the input of the integrator 3 in which the limited signal is integrated so that the original input signal is again obtained at the output of the ingegrator 3, while noise components are eliminated or suppressed.

The detailed circuit diagram of the conventional limiter circuit shown in Figure 1 is shown in Figure 2. Each block in Figure 1 is shown by dot-dash lines in Figure 2. The amplitude limiter circuit 2 comprises two diodes and two sources of predetermined

voltages $E_1$ and $E_2$. It will be understood that the limiter circuit is a combination of two clipping circuits each of which consists of a series circuit of a diode and a source of a predetermined voltage. The differentiator 1 produces a differentiated signal in response to the input signal and this differentiated signal is applied to the amplitude limiter 2. The negative voltage of the differentiated signal is limited at a voltage $-E_1$, while the positive voltage of the same differentiated signal is limited at a voltage $+E_2$. This means that the amplitude of the output of the limiter circuit 2 is limited within a predetermined range defined by the upper and lower limits $+E_2$ and $-E_1$. When the conventional noise limiter circuit shown in Figure 2 is used in an AM radio receiver, the following drawback is inevitable.

The amplitude of the detected signal of an AM signal is apt to remarkably vary in accordance with the variation of the magnitude (field intensity) of the receiving signal. However, since the threshold voltages (the above mentioned upper and lower limits $+E_2$ and $-E_1$) of the amplitude limiter 2 are fixedly determined, by constant voltages, the amplitude of the signal component per se may be erroneously limited when the magnitude of the input signal is relatively great. For instance, if the magnitude of the receiving signal of the AM radio receiver is great, the magnitude of the detected signal is also great accordingly. When such a detected signal is fed to the differentiator 1, the magnitude of the differentiated signal is also great. In such a case, if the amplitude of the differentiated signal is greater than the limiting range of the amplitude limiter 2, some portion of the differentiated signal is undesirably eliminated, causing occurrence of distortion in the integrated signal. Therefore, if it is desired to reduce such distortion, the limiting range of the amplitude limiter 2 has to be set at a relatively large value. However, it will be recognized that the larger limiting range results in low efficiency of the suppression of the noise components.

According to the present invention, the limiting range of the amplitude limiter is not fixedly set, but is arranged to vary in accordance with the magnitude of the input signal. In other words, the limiting range is made larger and larger as the magnitude of the input signal increases.

Referring to Figure 3, a schematic block diagram of a preferred embodiment of the limiter circuit according to the present invention is illustrated. In Figure 3, the limiter circuit is shown to be used in a conventional AM radio receiver. The radio receiver comprises an antenna 11, a radio frequency amplifier stage 12, a local-oscillator and mixer stage 13, an intermediate frequency amplifier stage 14, a detector stage 15, an audio frequency amplifier stage 16, and a speaker 17. The noise limiter circuit generally depicted by a reference number 9 is interposed between the detector stage 15 and the audio frequency amplifier stage 16 and comprises a differentiator 18, an amplitude limiter 19 and an integrator 20. The noise limiter circuit 9 further comprises a threshold voltage generating circuit generally depicted by a reference numeral 10.

Although the combination of the differentiator 18, the amplitude limiter 19 and the integrator 20 is the same in construction as the conventional noise limiter circuit as shown in Figure 1, the threshold voltages of the amplitude limiter 19 is controlled in accordance with the output voltages of the threshold voltage generating circuit 10. The threshold voltage generating circuit 10 includes a level detector 21 and a voltage control circuit 22. The level detector 21 produces an output signal indicative of the amplitude of the input signal of the noise limiter circuit 9. In this embodiment, the level detector 21 is arranged to be responsive to the voltage of the intermediate frequency signal derived from the intermediate frequency amplifier stage 14. Of course other signal, such as an AGC (automatic gain control) signal, which represents the magnitude of the input signal of the limiter circuit 9 may be used in place of the intermediate frequency signal.

The voltage control circuit 22 produces a bias voltages which will be used as threshold voltages in the amplitude limiter 19. The bias voltages are arranged to vary in accordance with the voltage of the output signal of the level detector 21. The threshold voltage generating circuit 10 has an input-output characteristic as shown in Figure 4. The co-ordinate shown in Figure 4 has an abscissa along which the voltage V of the input signal of the level detector 21 is plotted and an ordinate along which the threshold voltages $V_t$ produced by the voltage control circuit 22 are plotted. As shown the absolute values of the threshold voltages $V_t$ increase as the voltage V of the input signal increases. The hatched portion between the two (upper and lower) threshold voltages indicates an area in which the amplitude of the input signal of the limiter circuit 9 is not limited. In other words, signal components residing in this hatched area are transmitted via the amplitude limiter 19 without any suppression.

It will be understood that undesirable distortion does not occur since the threshold voltages, in absolute value, increase as the input voltage of the limiter circuit 9 increases. Although the efficiency of the suppression of noise components diminishes to an extent when the voltage V of the input signal is high, the noise component included in the signal is masked by the signal component, and therefore, the noise component does not cause trouble since the magnitude of the noise output is negligibly small in view of the auditory sensation.

Generally speaking, in an AM radio receiver mounted in a vehicle, such as a motor car, an impulsive noise, for instance the ignition noise emitted from the ignition system of an internal combustion engine, does not cause trouble when the field intensity of the receiving signal is relatively high. However, when the field intensity of the receiving signal is relatively low, or when the receiving frequency is detuned, the noise may be jarring to the listener's ear. It will be understood that according to the present invention, as the threshold voltages of the amplitude limiter 9 have clipping characteristics as shown in Figure 4, the high S/N (signal to noise) ratio is maintained irrespectively of the field intensity of the receiving signal.

Reference is now made to Figure 5 which shows a

detailed circuit diagram of the noise limiter circuit 9 shown in Figure 3. Elements in Figure 5 are enclosed by dot-dash lines to show the correspondency with the each block in Figure 3. The limiter circuit 9 has an input terminal IN, an output terminal OUT and a control terminal IF. The differentiator 18 comprises an operational amplifier $IC_3$ having inverting and noninverting inputs (−) and (+). The differentiator 18 further comprises two capacitors $C_4$ and $C_5$ and five resistors $R_{11}$ to $R_{15}$. The input terminal IN, via which an input signal, such as the detected signal from the detector 15 shown in Figure 3, is applied to the limiter circuit 9, is connected via a series circuit of a resistor $R_{11}$, a capacitor $C_4$ and another resistor $R_{12}$, to the inverting input (−) of the operational amplifier $IC_3$. The noninverting input (+) of the operational amplifier $IC_3$ is connected via a resistor $R_{15}$ to a junction connecting two resistors $R_{16}$ and $R_{17}$ which constitute a voltage divider provided between a power supply $V_{cc}$ and ground. A capacitor $C_5$ is interposed between a junction connecting the resistor $R_{11}$ and the capacitor $C_4$, and the inverting input (−) of the operational amplifier $IC_3$, while a resistor $R_{13}$ is connected across the inverting input (−) and the output of the operational amplifier $IC_3$. The output of the operational amplifier $IC_3$ is connected via a resistor $R_{18}$ to a cathode of a diode $D_2$ and to an anode of another diode $D_3$ included in the amplitude limiter 19. Although the amplitude limiter 19 is shown to have an input and an output in Figure 3, the actual input and output are the same since the amplitude limiter 19 consists of two diode clipping circuits. The anode of the diode $D_2$ and the cathode of the other diode $D_3$ are respectively connected to the outputs of the voltage control circuit 22 which will be described in detail hereinafter. The output of the amplitude limiter 19 is connected to an input of the integrator 20 which includes a resistor $R_{19}$ and a capacitor $C_6$. A junction between the resistor $R_{19}$ and the capacitor $C_6$ is connected to the output terminal OUT of the noise limiter circuit 9. This output terminal OUT may be connected to the input of the audio frequency amplifier stage 16 shown in Figure 3 when the noise limiter circuit 9 is used in AM radio receiver.

The level detector 21 comprises three capacitors $C_1$, $C_2$ and $C_3$, a resistor $R_{10}$ and a diode $D_1$. The control terminal IF of the amplitude limiter 9 is an input of the level detector 21 for receiving a signal, such as the intermediate frequency signal of a radio receiver, indicative of the magnitude of the detected signal. The input terminal IF of the level detector 21 is connected via the capacitor $C_2$ to the cathode of the diode $D_1$ the anode of which is connected via a capacitor $C_3$ to ground. The cathode of the diode $D_1$ is connected via a series circuit of a resistor $R_{10}$ and a capacitor $C_1$ to the anode of the same diode $D_1$, while the anode of the diode $D_1$ is connected to the junction between the resistors $R_{16}$ and $R_{17}$.

The voltage control circuit 22 includes first and second operational amplifiers $IC_1$ and $IC_2$, and resistors $R_1$ to $R_9$. A junction connecting the resistor $R_{10}$ and the capacitor $C_1$ is connected via a resistor $R_3$ to an inverting input (−) of the first operational amplifier $IC_1$ included in the voltage control circuit 22. The junction between the resistors $R_{16}$ and $R_{17}$ is further connected via resistors $R_4$ and $R_7$ to the noninverting inputs (+) of the first and second operational amplifiers $IC_1$ and $IC_2$. The inverting input (−) of the first operational amplifier $IC_1$ is connected via a resistor $R_1$ to ground, and is further connected via a resistor $R_2$ to the output of the first operational amplifier $IC_1$. The output of the first operational amplifier $IC_1$ is connected via a resistor $R_8$ to ground. The inverting input (−) of the second operational amplifier $IC_2$ is connected via a resistor $R_5$ to the output of the first operational amplifier and is further connected via a resistor $R_6$ to the output of the second operational amplifier $IC_2$. The output of the second operational amplifier $IC_2$ is connected via a resistor $R_9$ to ground. The outputs of the first and second operational amplifiers $IC_1$ and $IC_2$ are respectively connected to the anode of the diode $D_2$ and the cathode of the other diode $D_3$ both included in the amplitude limiter 19.

The limiter circuit shown in Figure 5 operates as follows. The input terminal IF (controlled terminal) of the level detector 21 is responsive to the intermediate frequency signal or the AGC signal derived from the intermediate frequency amplifier stage 14. Since the diode $D_1$ functions as a half-wave rectifier, a DC voltage proportion to the amplitude of the input signal (IF signal) applied to the input IF is developed across the capacitor $C_1$. Meanwhile, one terminal of the capacitor $C_1$ is supplied with a predetermined voltage $V_0$ from the voltage divider ($R_{16}$ and $R_{17}$) and therefore, the voltage $V_{DC}$ at the junction between the resistor $R_{10}$ and the capacitor $C_1$ varies with respect to this predetermined voltage $V_0$.

The predetermined voltage $V_0$ will be used in the following stage, i.e. the voltage control circuit 22, as a reference voltage, while the variable DC voltage $V_{DC}$ is applied to a first inverting amplifier constituted by the first operational amplifier $IC_1$ and resistors $R_1$ to $R_4$. The first inverting amplifier produces an output voltage at the output of the first operational amplifier $IC_1$, wherein the output voltage is expressed in terms of $V_0 - V_{DC}$. A second inverting amplifier consisting of the second operational amplifier $IC_2$ and resistors $R_5$ to $R_7$ is responsive to the output voltage of the first inverting amplifier and to the predetermined voltage $V_0$. Therefore, the second inverting amplifier produces an output voltage at the output of the second operational amplifier $IC_2$, wherein the output voltage is expressed in terms of $V_0 + V_{DC}$. These two voltages $V_0 - V_{DC}$ and $V_0 + V_{DC}$ are respectively supplied to the anode of the diode $D_2$ and to the cathode of the diode $D_3$ as biase voltages.

With this arrangement, the threshold voltages (clipping levels) of the amplitude limiter 19 are respectively set at these voltages determined by the voltage control circuit 22. This means that the amplitude limiter 19 has a limiting range of $\pm V_{DC}$ with respect to the reference voltage $V_0$. In other words, the width of the limiting range equals $2V_{DC}$. Of course the width of the limiting range may be variable by means of adjustment of the amplification degree of the first and second inverting amplifiers.

Turning back to Figure 3, let us assume that the

AM radio receiver is tuned at a specific radio wave. The radio wave catched by the antenna 11 is amplified by the radio frequency amplifier stage 12 and then converted into an intermediate frequency via the local oscillation/mixer stage 13. The intermediate frequency is amplified in the intermediate frequency amplifier stage 14 to be supplied to the following detector stage 15. The radio receiver comprises an AGC circuit which controls the amplification degree of various stages in accordance with the magnitude of the received signal. Assuming that the field intensity of the radio wave to be received increases, the amplitude of the detected signal derived from the detector 15 increases accordingly. At this time, the magnitude of the intermediate frequency signal and the AGC signal derived from the intermediate frequency amplifier stage 14 increase in the same manner. The intermediate frequency signal or the AGC signal supplied to the control terminal IF is rectified by the diode $D_1$ included in the level detector 21. The voltage $V_D$ across the capacitor $C_1$ increases in proportion to the increase of the voltage of the AGC signal. Two bias voltages $V_0 - V_{DC}$ and $V_0 + V_{DC}$ will be produced by the first and second inverting amplifiers in accordance with the voltage $V_{DC}$ across the capacitor $C_1$.

From the foregoing, it will be understood that the limiting range ($2 V_{DC}$) of the amplitude limiter 19 varies in accordance with the voltage V of the input signal of the level detector 21 as shown in Figure 4. The differentiated signal obtained at the output of the differentiator 18 is thus limited within this limiting range defined by the bias voltages $V_0 - V_{DC}$ and $V_0 + V_{DC}$ so that undesirable impulsive noise is eliminated from the differentiated signal. This signal is integrated by the integrator 20 which follows the amplitude limiter 19. Consequently, the input signal of the differentiator 18 is restored to the original state at the output of the integrator 20, while the impulsive noise components are removed.

Figure 6A to 6C show the results of experiments in connection with the noise limiter circuit according to the present invention. In Figure 6A, the waveform of an input impulsive noise is shown by a curve A, while the waveform of the same impulsive noise through the noise limiter circuit according to the present invention is also shown by a curve b. As shown, when the magnitude of the input impulsive noise is 90 mili volt and the pulse width is 200 micro second, the output voltage of the noise limiter circuit is 20 mili volt. This means that the degree of suspression of an impulsive noise component is approximately 15 dB. Figure 6B shows the waveform of a detected output signal delivered in receipt of a carrier input signal (1 M Hz, 65 dB, the modulation frequency: 1 K Hz, the modulation degree: 30 per cent) which includes the above described impulsive noise component, which detected output signal will be fed to the noise limiter circuit. Upon receiving the detected output signal shown in Figure 6B, the noise limiter circuit according to the present invention produces an output signal the waveform of which is shown in Figure 6C. As will be seen in Figure 6C, the output signal derived from the noise limiter circuit includes negligible noise components, and is substantially same as the modulation frequency.

CLAIMS:-

1. A noise limiter circuit including:

(a) a differentiator responsive to an input signal for producing a differentiated signal;

(b) an amplitude limiter responsive to said differentiated signal for limiting the amplitude of said differentiated signal; and

(c) an integrator responsive to the output signal of said amplitude limiter for restoring the original input signal where the noise components included in the input signal are suppressed; wherein the improvement comprises:

means for providing said amplitude limiter with variable threshold voltages, which are arranged to vary in accordance with the magnitude of said input signal.

2. A noise limiter circuit as claimed in Claim 1, wherein said means comprises a level detector responsive to the magnitude of said input signal for producing an output signal proportional to said magnitude; and a voltage control circuit responsive to said output signal of said level detector for producing first and second threshold voltages of opposite polarity.

3. A noise limiter circuit as claimed in Claim 2, wherein said level detector comprises a rectifier for producing a DC signal the voltage of which is proportion to the input signal and a capacitor responsive to said DC voltage for storing said DC voltage therein.

4. A noise limiter circuit as claimed in Claim 3, wherein said voltage control circuit comprises first and second inverting amplifiers, said first inverting amplifier being responsive to the voltage of said capacitor and a predetermined reference voltage, said second inverting amplifier being responsive to the output voltage of said first inverting amplifier and said predetermined reference voltage, the output voltages of said first and second inverting amplifiers being used as said threshold voltages of said amplitude limiter.

5. A noise limiter circuit as claimed in Claim 1, wherein said means is arranged to be responsive to the intermediate frequency signal of a radio receiver.

6. A noise limiter circuit as claimed in Claim 1, wherein said means is arranged to be responsive to the automatic gain control signal of a radio receiver.

7. A noise limiter circuit substantially as hereinbefore described with reference to the accompanying drawings Figure 3 to Figure 6C.

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